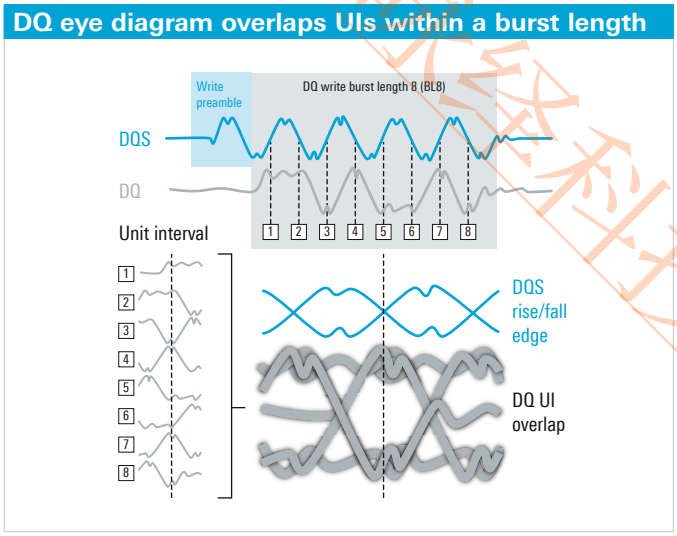
DDR3 data eye diagram testing

Compliance testing is essential to ensure that dynamic random access memory (DRAM) signals meet specifications in timing, slew rates and voltage levels. To quickly check signal qualities, eye diagram testing can provide insights into signal integrity conditions in a much shorter time.



Your task

When testing DDR interface signal quality, data eye analysis helps to reveal potential signal integrity issues. Therefore, the eye diagram function is very popular among many SI engineers because it enables them to quickly determine DDR interface performance. While compliance tests verify signal characteristics of data, address, control and clock signal groups in detail in line with JEDEC specifications, they lack the flexibility to debug signal integrity issues quickly. The main challenge for eye diagram testing is the need of read/write separation as well as overlapping consecutive bits within the data bursts in order to test them based on simple masks.

Rohde&Schwarz solution

The R&S®RTx-K91 DDR3 signal integrity and compliance test software option features comprehensive DDR3 compliance test software that includes an additional DDR eye diagram function for signal integrity debugging. The option also offers the capability to identify read and write bursts by decoding them using data and strobe phase difference and signal level.

The DDR eye

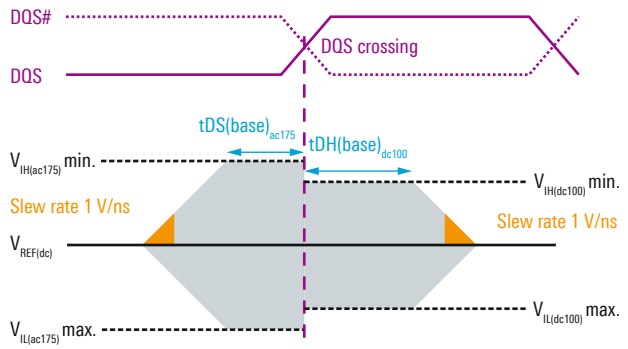
Unlike many other high-speed interfaces, JEDEC's DDR3 specification does not require an eye diagram test; it is used to validate the signal quality but does not provide mask information. A DDR read/write data burst includes a preamble bit that could mess up creating a simple eye when just using DQS strobe as the timing alignment.

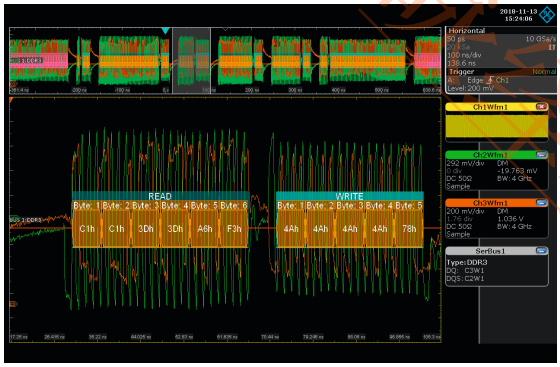
The R&S®RTx-K91 option also uses DQS rising and falling edges to align different transitions of DQ signals, but it intelligently omits the preamble bit prior to the data burst to form a proper eye diagram suitable for testing.

Mask test and limit

A DDR3 mask can be derived from the JEDEC specification: data setup (tDS) and hold time (tHD) define the width of the eye; slew rates, input and output voltage level define the vertical eye opening. This methodology to construct the mask can be used for quickly testing the signal integrity. Note that in the DDR3 specification, the signal timing and level requirement depend on the actual signal slew rates as well as the selected reference level and data rates. Therefore, the user will need to define the mask that fits the device characteristic and apply a proper configuration.

Example of defining an eye mask for DDR3

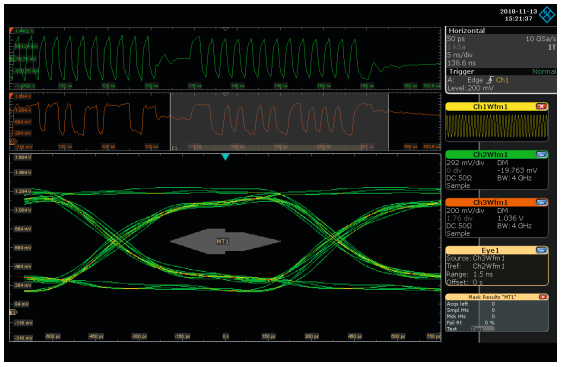




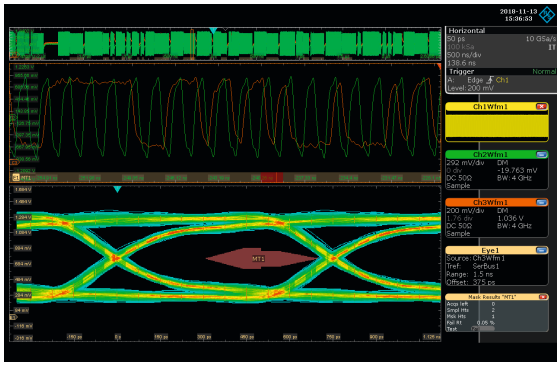
Using DQ and DQS to determine the read/write burst

The R&S®RTO and R&S®RTP oscilloscope standard mask test function works together with the R&S®RTx-K91 DDR3 eye diagram tool. Users can define required mask profiles and save them for later testing. Violations of the mask are indicated on the waveform (eye stripe function) and can be tabulated based on UI sequences. Users zoom into individual violations to further analyze and debug signal integrity issues.

Decoding simplifies identification of read/write bursts solely based on DQ and DQS phase relationship and threshold hysteresis without the need of probing additional control signals. Users capture a longer duration of DQ bursts to create a write and/or read-only eye diagram for testing. Once an eye diagram is established, analysis tools such as mask test, histogram and automated eye measurements can be applied.



R&S®RTP-K91 eye diagram mask test on gated burst



Testing write cycles with mask test indication violation area

Separating read/write bursts

Advanced triggering methods such as evaluating DQ/DQS phase, using an MSO's logic probes on a command bus or even zone triggering can help to differentiate read/write cycles. However, only capturing the signal using a dedicated trigger will limit the visibility to signal anomalies not defined in the trigger condition. Therefore, the R&S®RTx-K91 option comes with a decoding function that helps to distinguish all read/write cycles in the acquired waveforms.

Summary

In DRAM DDR3 interface testing, compliance tests help to benchmark the interoperability against the JEDEC standard. When debugging SI issues, features and tools such as mask test, eye diagram tool and read/write separation are needed to facilitate the analysis effort. The R&S®RTx-K91 option therefore offers the full compliance and debugging arsenal for DDR3 testing.

Ordering information

Designation	Type	Order No.
High-performance oscilloscope, 8 GHz, 4 channels	R&S®RTP084	1320.5007.08
Oscilloscope, 4 GHz, 4 channels	R&S®RTO2044	1329.7002.44
DDR3 signal integrity and compliance test software	R&S®RTP-K91	1337.8840.02
DDR3 signal integrity and compliance test software	R&S®RTO-K91	1337.8891.02

Rohde&Schwarz GmbH&Co. KG
Europe, Africa, Middle East | +49 89 4129 12345
North America | 1 888 TEST RSA (1 888 837 87 72)
Latin America | +1 410 910 79 88
Asia Pacific | +65 65 13 04 88
China | +86 800 810 82 28 | +86 400 650 58 96
www.rohde-schwarz.com
customersupport@rohde-schwarz.com

PD 5216.4733.92 | Version 01.00 | February 2019 (sk)
DDR3 data eye diagram testing
Data without tolerance limits is not binding | Subject to change

5216473392

5216.4733.92 01.00 PDP 1 en